WHAT IS CLAIMED IS:

1. An image processing apparatus which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus comprising:

an input I/F memory which reads pixels having a predetermined length, subjects these pixels to buffering, and then writes these pixels in a SIMD type processor;

a SIMD type processor which performs batch processing of the pixels written from said input I/F memory;

an output I/F memory which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes the pixels in a predetermined output destination; and

a control unit which controls the read and/or write timing of said input I/F memory and said output I/F memory.

2. The image processing apparatus according to claim 1, wherein said control unit controls the write and/or read timing to thereby use said input I/F memory and output I/F memory a plurality of times.

3. The image processing apparatus according to claim 1, wherein an effective number of pixels obtained by subtracting the number of peripheral pixels referred to for

said target pixel from the number of pixels batch-processed by said SIMD type processor is multiples in a dither matrix.

4. The image processing apparatus according to claim 1, wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.

5. An image processing apparatus which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus comprising:

an input I/F memory which reads pixels having a predetermined length, subjects these pixels to buffering, and then writes these pixels in a SIMD type processor at a speed faster than when the pixel were read;

a SIMD type processor which performs batch processing of the pixels written from said input I/F memory;

an output I/F memory which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes these in a predetermined output destination at a speed slower than that of readout of said batch-processed pixels; and

a control unit which controls the read and/or write timing and read and/or write speed of said input I/F memory and said output I/F memory.

6. The image processing apparatus according to claim 5, wherein said control unit controls the write and/or read timing to thereby use said input I/F memory and output I/F memory a plurality of times.

7. The image processing apparatus according to claim 5, wherein an effective number of pixels obtained by subtracting the number of peripheral pixels referred to for said target pixel from the number of pixels batch-processed by said SIMD type processor is multiples in a dither matrix.

8. The image processing apparatus according to claim 5, wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.

9. An image processing apparatus which refers to peripheral pixels of a target pixel to perform processing of said target pixel, said image processing apparatus comprising:

an input I/F memory which reads pixels having a predetermined length, subjects these pixels to buffering, and then writes these pixels in a SIMD type processor at a speed faster than when the pixels were read, and which has a capacity smaller than pixels batch-processed by said SIMD type processor;

a SIMD type processor which performs batch processing of the pixels written from said input I/F memory;

an output I/F memory which reads the pixels batch-processed by said SIMD type processor, subjects the pixels to buffering and writes these in a predetermined output destination at a speed slower than when the batch-processed pixels were read, and which has a capacity smaller than pixels batch-processed by said SIMD type processor; and

a control unit which controls the write and/or read speed with respect said input I/F memory, and the write and/or read timing with respect said input I/F memory based on said speed and the capacity of said input I/F memory, and/or the write and/or read speed with respect said output I/F memory, and the write and/or read timing with respect said output I/F memory based on said speed and the capacity of said output I/F memory.

10. The image processing apparatus according to claim 9, wherein said control unit controls the write and/or read timing to thereby use said input I/F memory and output I/F memory a plurality of times.

11. The image processing apparatus according to claim 9, wherein an effective number of pixels obtained by subtracting the number of peripheral pixels referred to for

said target pixel from the number of pixels batch-processed by said SIMD type processor is multiples in a dither matrix.

12. The image processing apparatus according to claim 9, wherein said SIMD type processor is physically detachable from said input I/F memory or said output I/F memory.